IB04/03407

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Patentanmeldung Nr. Patent application No. Demande de brevet n°

03300175.1

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Europäisches Patentamt
European Patent Office
Office européen des brevets

Anmeldung Nr:
Application no.: 03300175.1
Demande no:

Anmeldetag:
Date of filing: 22.10.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
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A method and a system for powering an integrated circuit, and an integrated circuit especially designed to be use therein

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL
PT RO SE SI SK TR LI

Description

Field of the invention:

The present invention relates to a method and a system for powering an integrated circuit, said integrated circuit comprising a die within a package assembly, the die comprising a plurality of logic circuits, each of the logic circuit having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage.

More precisely, the invention relates to a method for powering an integrated circuit comprising the steps of :

- measuring the power voltage supplied to the integrated circuit, and
- regulating this power voltage in order to maintain the difference between the measured voltage and a reference voltage as small as possible.

The invention also relates to an integrated circuit especially designed to be used in the above method.

It is known that to design a faster integrated circuit that executes operations more rapidly, one solution is to build the integrated circuit using faster logic circuits. However, faster logic circuits are bigger than normal logic circuits. So this solution results in integrated circuits having increased size.

Another solution is to increase the power voltage of the integrated circuit. Indeed, the higher the power voltage is, the faster the integrated circuit is.

However, in no case the power voltage should exceed a nominal maximum operating voltage, otherwise this may result in the integrated circuit being definitely damaged.

In order to power the integrated circuit with a voltage as close as possible to its nominal maximum operating voltage, power supply system with active feedback are used.

Such systems are also known as "remote sensing" circuits.

According to typical prior systems, active feedback is used by power supplies to compensate for voltage drops due to the impedances of the conductors via

which power is transmitted to a load, which may be an integrated circuit. A power supply may include circuitry that compensates for such voltage drops by remotely sensing the voltage delivered to the load. The sensed voltage is typically compared to a voltage reference of the power supply. If the voltage at the integrated circuit is different from the voltage reference, the power supply adjusts its output power voltage, either upwards or downwards, until the sensed voltage is equal to the voltage reference.

As a practical matter, the nominal maximum operating voltage for an integrated circuit as specified by the manufacturer of the integrated circuit is typically under the actual maximum operating voltage of the integrated circuit by an operating margin voltage, wherein the maximum operating voltage is the voltage level above which the transistors or logics of an integrated circuit will be damaged. To better ensure continuous operation of the integrated circuit under different operating conditions, the manufacturer of the integrated circuit selects the operating margin voltage by taking into consideration a theorized minimum voltage drops inside the die of the integrated circuit and a theorized minimum voltage drops at the electrical interface with the die. The value of the operating margin voltage is also selected to account for inaccuracies of the testing equipment that rates the maximum voltage at which the integrated circuit continue to operate.

Voltage drops in the die of the integrated circuit are often referred to as "on-chip losses" and include voltage drops due to the inherent impedances of the semiconductor material from which the die is manufactured. On-chip losses can vary for each semiconductor die manufactured according to the same integrated circuit design. The actual on-chip losses of a particular semiconductor die may, in fact, be much more than the best-case on-chip losses that are accounted for by the operating margin voltage, which means that the voltage supplied to such a semiconductor die could be increased above the nominal maximum operating voltage if the actual on-chip losses were known.

Voltage drops at the electrical interface with the die of the integrated circuit are often referred to as "package losses" and include voltage drops due to the impedance of the bond wires, the impedance of the package leads, the interface between the bond wires and the semiconductor die, the interface between the bond wires and the package leads, and the interface between the leads of a package and the printed circuit board. Like on-chip losses, the actual package losses of a particular semiconductor die may be worst than the best-case package losses that are accounted for by the operating margin

voltage, which means that the voltage supplies to such a semiconductor die could be increased-above the nominal maximum operating voltage if the actual package losses were known.

Therefore, the method using remote sensing or other known methods are not optimal.

Summary of the invention

It is accordingly an object of the invention to provide a method to power each integrated circuit with a voltage very close to its actual maximum operating voltage.

With the foregoing and other objects in view there is provided in accordance with the invention, a method wherein during the measuring step the power voltage is directly measured within the die at the power input of at least one of the logic circuits, and wherein the method comprises the step of setting the reference voltage so that the voltage supplied to the power input of at least one logic circuit of the die is equal to the predetermined maximum operating voltage of this logic circuit.

In the above method, the voltage used to regulate the power voltage supplied to the integrated circuit is directly measured within the die of the integrated circuit and therefore by-passes at least the package losses. So, the regulated voltage supplied to the integrated circuit is automatically adjusted upward in order to compensate for the actual package losses.

Therefore, the voltage supplied to the integrated circuit according to the above method is higher than the one supplied according to the known method and the integrated circuit operates at higher speed than previously.

The features as defined in claims 2 to 3 have the advantage that the method also compensate for the on-chip losses.

The features as defined in claim 4 have the advantage that the method can be used with already existing integrated circuit.

Other features of the claim invention are recited in the dependant claims.

The invention also concerns a system to power an integrated circuit according to the above method.

The invention also concerns an integrated circuit especially designed to be powered according to the above method and having a sense point at the power input of

the first logic circuit that would be damaged in case of voltage increase over the predetermined maximum operating voltage of this logic circuit.

Brief description of the drawings

Fig.1 is a cross-section of an integrated circuit,

Fig.2 is a schematic diagram of a system for remote sensing according to the invention, and

Fig.3 is a flow chart of a method for powering an integrated circuit according to the invention.

Description of the prefered embodiments

Fig.1 shows a cross-section of an integrated circuit 2. This integrated circuit may be a microprocessor, a memory circuit or the likes.

Integrated circuit 2 comprises a semiconductor die 4 within a package assembly 6.

Semiconductor die 4 is connected to package leads 8 via bond-wires 10. Each bond-wire is connected at one end to one package lead 8 and at the other end to a bond pad 12.

Here, bond pads 12 are intended to receive voltage supplied by a power supply through the package leads 8.

Die 4 comprises a great number of logic circuits. Each logic circuit has a positive power input, which is connected to pad 12 through conductive traces in order to be supplied with a positive voltage.

Hereinafter, the term "logic circuit" will be understood to refer to any logic device or circuit which, when implemented at the transistor level, includes at least a positive power input. Such a logic circuit may be, for example, logic gates such as OR gates, AND gates, NOR gates, NAND gates,...etc, or N channel and P channel transistors.

To simplify Fig.1, only two logic circuits 16 and 18 which are connected to pad 12 via conductive traces 20 and 22 (Fig.2), respectively, are represented.

Fig.2 shows a remote sensing system 30 that comprises a power supply 32 with a regulating circuitry 33, which is connected to integrated circuit 2. Elements of integrated circuit 2 that have already been described in regard of figure 1 are designed using the same numeral references.

Power supply 32 includes a V_{CC} output pin 34, which supplies the power voltage V_{CC} to lead 8 via a supply line 36.

Power supply 32 also includes a V_{SS} output pin which supplies a system ground voltage V_{SS} to a package lead 40 of integrated circuit 2 via a ground line 42. Package lead 40 is connected via one bond wire to a bond pad 44 to which ground input voltage of each logic circuit is connected.

Power supply 32 also includes a sense input pin 50 and a V_{ref} input pin 52.

Input pin 50 is connected to a sense package lead 54 of the integrated circuit 2 via an input line 56.

Sense lead 54 is connected to a bond pad 58 of the die 4 via a bond wire 60. Bond pad 58 is connected to a sense point 61 via a conductive trace 62. Sense point 61 is placed within die 4 at the power input of the logic circuit which is known to be the first to be damaged in case of power voltage increase. This will be explained in more details in regard of figure 3.

The input impedance of input pin 50 is very large so the conduction path from sense line 56 to sense pin 50 appears to be an open circuit and little or no current flows through sense line 56. Therefore, there is virtually no on-chip or package losses due to the impedance of bond wire 60 and trace 62.

Pin 52 is connected to a constant reference voltage V_{ref}. Reference voltage V_{ref} is set to be equal to the predetermined maximum operating voltage of logic circuit 16. The predetermined maximum operating voltage of a logic circuit is determined by the manufacturer during the design process of die 4. Typically the predetermined maximum operating voltage of a logic circuit is higher than the nominal maximum operating voltage of the integrated circuit 2 since on-chip losses and package losses are not taken into consideration for its determination.

The way in which the remote sensing system 30 is designed and works will now be explained in regard of figure 3 in the particular case in which every logic circuit of die 4 have a same predetermined maximum operating voltage equal to 1.2V.

During design, in step 80, of the integrated circuit 2, a conductive trace is routed from each power input of each logic circuit to bond pad 12. The impedances of each of these traces are not the same. Indeed, for example, the impedance of trace 22 will be higher that the impedance of trace 20 since trace 22 is longer than trace 20. Therefore, the voltage V_I at the power input of logic circuit 16 will be higher than the

voltage V_2 at the power input of logic circuit 18. Therefore, sense point 61 is placed within die 4 at the power input of the logic circuit associated with the lowest on-chip losses. In other words, this correspond here to the power input of the logic circuit which is designed to be supplied with the highest power voltage. Typically, the shortest power supply traces are the ones that connect logic circuits near the external periphery of die 4 to pad 12.

Here, as example, sense point 61 is placed, during an operation 82, at the power input of logic circuit 16.

Then, conductive trace 62 is routed during an operation 84, between sense point 61 and sense pad 58 and sense pad 58 is connected during an operation 86, to sense lead 54 via bond wire 60.

During a step 88 consisting of assembling remote sensing system 30, sense lead 54 is connected, during an operation 90, to input pin 50.

Then, the value of voltage reference V_{ref} of regulating circuitry 33 is set, during an operation 92, to be equal to the predetermined maximum operating voltage of logic circuit 16.

Once system 30 has been assembled, it works as follow.

At power on, the voltage V_{CC} supplied to lead 8 is low and under the predetermined maximum operating voltage of every logic circuit of the integrated circuit 2.

Then, the regulating circuit 33 regulates in step 96, the voltage V_{CC} so that the voltage V_1 is equal to reference voltage V_{ref}.

More precisely, the regulating circuitry measures, during an operation 98, the value of the voltage V_1 at sense point 61.

Then the measured voltage value is compared, during an operation 100, to the value of the reference voltage V_{ref}.

If the measured voltage V_1 is inferior to the value of reference voltage V_{ref}, then voltage V_{CC} is increased during step 102.

Otherwise, the regulating circuitry 33 maintains or decreases voltage V_{CC} during an operation 104.

After operation 102 or 104, the regulating circuitry 33 comes back to operation 98 in order to continuously regulate the voltage V_{CC} supplied to integrated circuit 2.

Since in system 30, integrated circuit 2 is powered at the predetermined maximum operating voltage of logic circuit 16, all logic circuits are operated at the maximum possible speed and integrated circuit 2 behaves faster than with known methods.

As an alternative, integrated circuit 2 may be replaced by the integrated circuit described in US 5 672 997. The integrated circuit disclosed in this document presents a sense lead connected to a sense point within the die in order to measure the lowest power voltage within the die of the integrated circuit.

If such an integrated circuit is used, operation 92 in figure 3 is replaced by two operations. The first one consists in establishing the value of the voltage drop due to the on-chip losses between the sense point and the power input of the logic circuit which is known to be the first to be damaged in case of power voltage increase. For example, if the sense point is placed at the power input of logic circuit 18, and the first logic circuit to be damaged is logic circuit 16, the voltage drop between voltages V_2 and V_1 is determined. Here, this voltage drop is assume to be equal to 0.1V.

The second operation consists in setting the value of reference voltage V_{ref} equal to the predetermined maximum operating voltage of logic circuit 16 minus the previously determined voltage drop. Therefore, according to this alternative embodiment, the value of voltage V_{ref} is set to 1.1 volt.

This alternative embodiment has the advantage to use the same sense lead as the one eventually used to minimize the power supply of such an integrated circuit. However, the voltage drop between voltages V_2 and V_1 cannot be established with a very high accuracy. So speed increase achieved with such an integrated circuit is not as good as with the integrated circuit 2 of the main embodiment.

Depending on the accuracy of regulating step 96, the value of the reference voltage V_{ref} may be set equal to a value under the predetermined maximum operating voltage of logic circuit 16 by an operating margin voltage in order to remain in every circumstances under this predetermined maximum operating voltage established during the designed of the integrated circuit design.

CLAIMS:

1. A method for powering an integrated circuit, said integrated circuit comprising a die (4) within a package assembly (6), the die comprising a plurality of logic circuits (16, 18), each of the logic circuit having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, the method comprising the steps of :

- measuring (in 98) the power voltage supplied to the integrated circuit, and
- regulating (in 96) this power voltage in order to maintain the difference between the measured voltage and a reference voltage as small as possible,
- wherein during the measuring step the power voltage is directly measured within the die at the power input of at least one of the logic circuits, and
- wherein the method comprises the step of setting (in 92) the reference voltage so that the voltage supplied to the power input of at least one logic circuit of the die is equal to the predetermined maximum operating voltage of this logic circuit.

2. The method according to claim 1, wherein during the step of measuring (in 98), the power voltage is measured within the die directly at the power input of the logic circuit known to be the first to be damaged in case of power voltage increase on at least one power input lead of the integrated circuit.

3. The method according to claim 2, wherein during the step of the measuring (in 98) the power voltage is measured within the die directly at the power input of the logic circuit known to be supplied with the highest power voltage available within the die.

4. The method according to claim 1, wherein, during the step of measuring (in 98), the power voltage is measured within the die directly at the power input of a first logic circuit, and wherein, during the step of setting, the reference voltage is set to the value of the predetermined maximum operating voltage of a second logic circuit known to be the first to be damaged in case of power voltage increase on at least one

power input lead of the integrated circuit minus a margin voltage representative of a voltage drop between the power inputs of the first and second logic circuits.

5. A powering system comprising :

- an integrated circuit (2) comprising a die (4) within a package assembly (6), the die comprising a plurality of logic circuits (16, 18), each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, and the package comprising at least one power input lead (8),

- a power supply (32) to supply a power voltage on said at least one power input lead (8), said power supply being able to regulate the power voltage supplied according to the difference between a reference voltage and a measured voltage at a sense point (61),

- wherein the sense point (61) is placed within the die (4) of the integrated circuit at the power input of one of the logic circuits (16), and

- wherein the reference voltage is set in order to supply to the power input of at least one logic circuit a voltage equal to the predetermined maximum operating voltage of this logic circuit.

6. The system according to claim 5, wherein the sense point (61) is placed at the power input of the logic circuit known to be the first to be damaged in case of power voltage increase on said at least one power input lead (8).

7. An integrated circuit comprising a die (4) within a package assembly (6), the die comprising a plurality of logic circuits (16, 18), each of the logic circuits having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage, the package assembly being provided with a plurality of leads (8, 5, 40, 54) to be connected to an external circuit board, one of these leads (54) being a sense lead to directly measure the voltage at a sense point (61) within the die and another lead being a power input lead (8), wherein the sense point (61) is placed at the power input of the logic circuit (16) known to be the first to be damaged in case of power voltage increase on the power input lead (8).

"A method and a system for powering an integrated circuit, and an integrated circuit especially designed to be used therein".

ABSTRACT

The method is for powering an integrated circuit, said integrated circuit comprising a die within a package assembly, the die comprising a plurality of logic circuits each of the logic circuit having at least one power input which should not receive a power voltage exceeding a predetermined maximum operating voltage. The method comprises the steps of:

- measuring (in 98) the power voltage supplied to the integrated circuit directly within the die at the power input of at least one logic circuit and
- regulating (in 96) this power voltage so that the voltage supplied to the power input of at least one logic circuit of the die is equal to the predetermined maximum operating voltage of this logic circuit.

Fig. 3

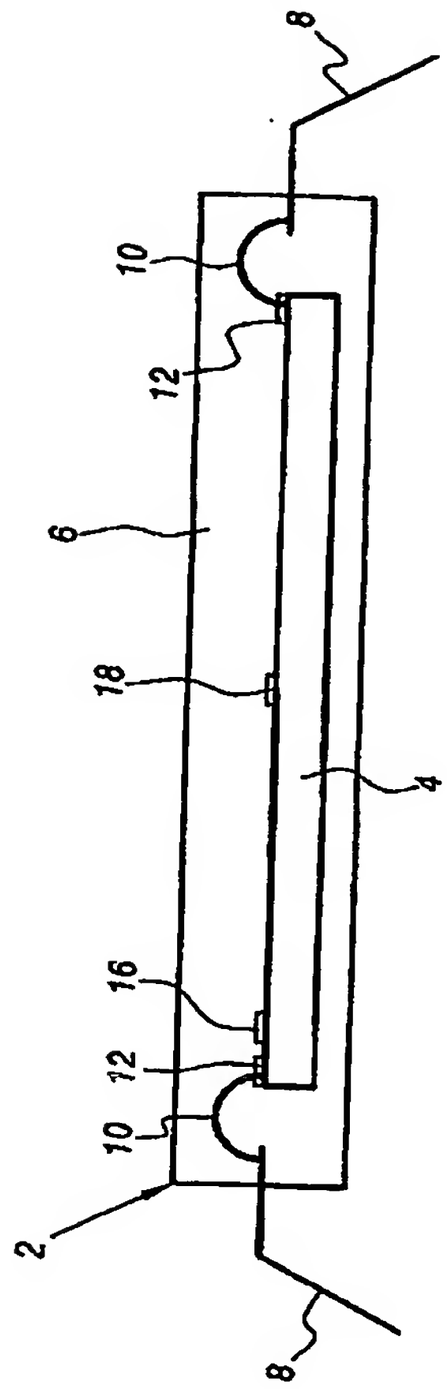

FIG.1

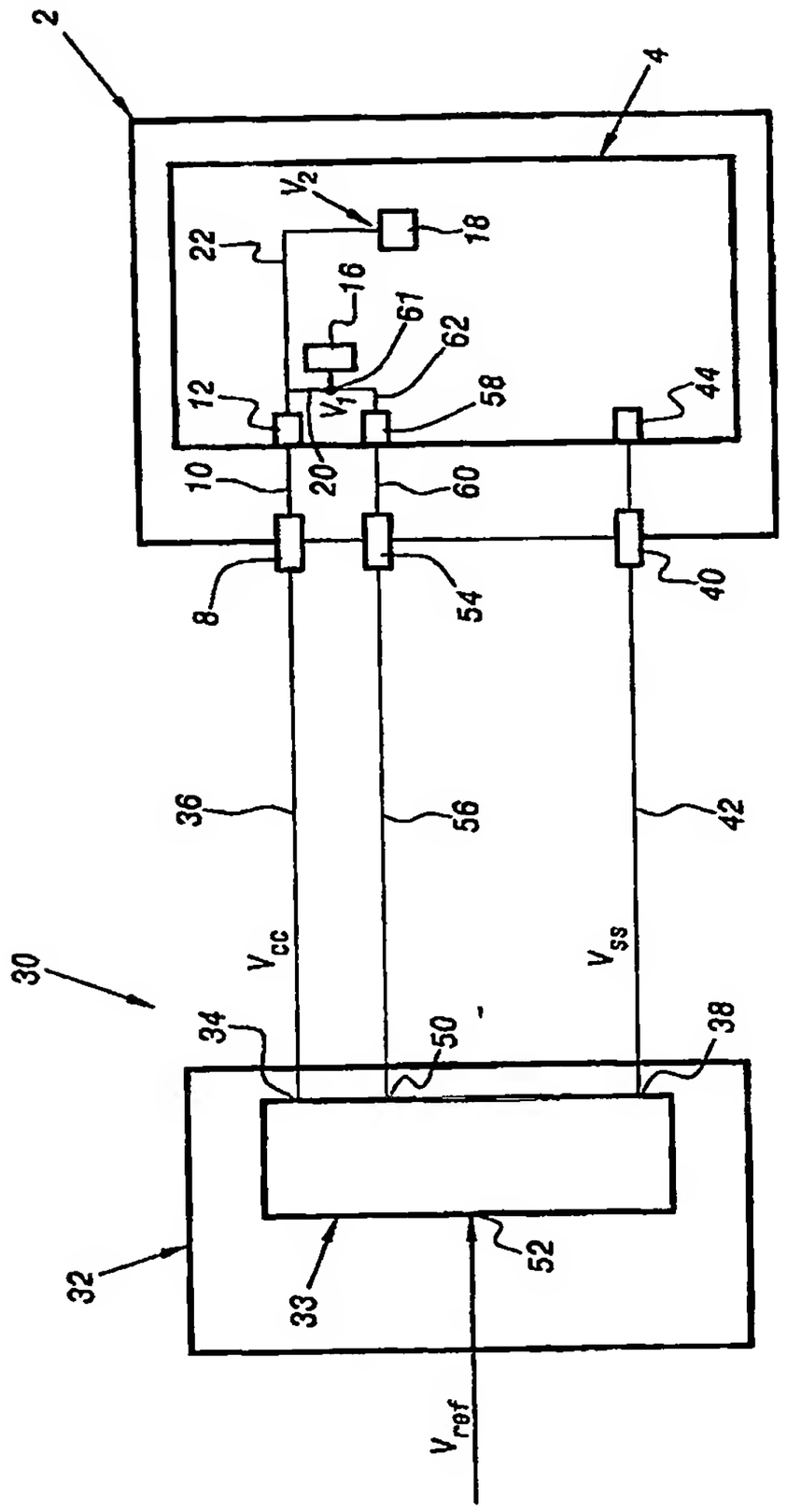
2
4
V_2
18
22
16
61
62
12
V_1
58
44
10
20
60
8
54
40
36
56
42
V_{cc}
V_{ss}
30
34
50
38
32
33
52
V_{ref}

FIG.2

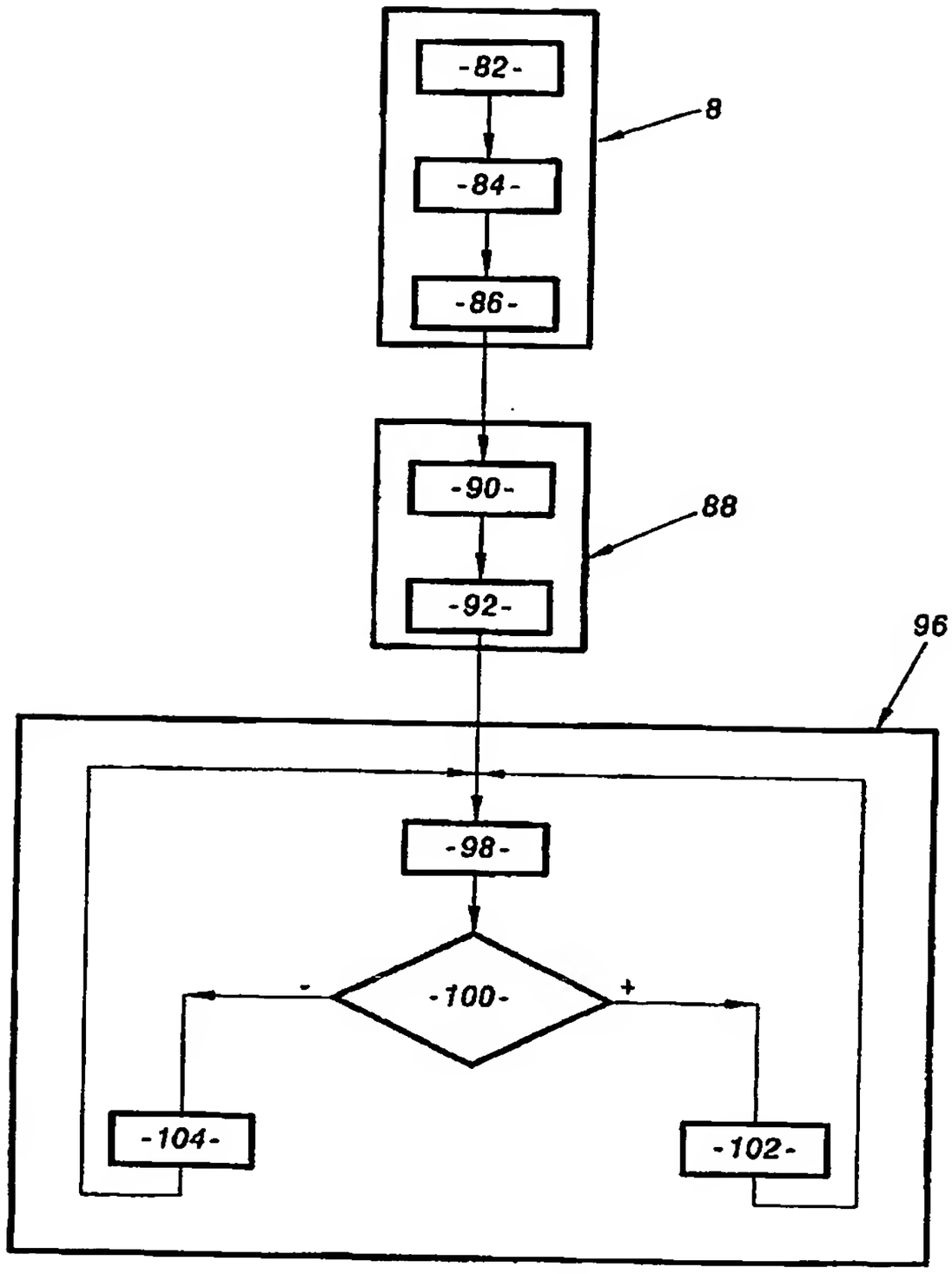

FIG.3